

**CLAIMS**

What is claimed is:

1. A method comprising:  
providing a register file accessible by a plurality of processing elements of a media signal processor;  
enabling a selected hardware accelerator from a plurality of hardware accelerators according to at least one bit of a register within the register file set by a processing element; and  
granting the processing element ownership over the selected hardware accelerator.
2. The method of claim 1, wherein enabling the selected hardware accelerator comprises:  
enabling a processing element to set a bit when the process desires selection of a hardware accelerator; and  
activating the selected hardware accelerator if the bit is set.
3. The method of claim 1, wherein enabling the selected hardware accelerator comprises:  
designating at least one register within the register file to receive control commands from the plurality of processing elements; and  
activating the selected hardware accelerator to perform a media processing function according to a control command detected within the register.
4. The method of claim 1, further comprising:  
providing a selection unit coupled to the plurality of hardware elements;  
designating at least one register within the register file to receive control commands from the plurality of processing elements;  
directing the selection unit to provide a processing element with access to a selected hardware element; and  
directing the selecting hardware accelerator to perform a media processing function according to a received control command.

5. The method of claim 3, wherein activating the selected hardware accelerator comprises:

- identifying a processing element having written the control command;
- determining, according to the control command, an input data stream for the selected hard accelerator;
- determining, according to the control command, an output data stream for the selected hard accelerator;
- directing the selecting hardware accelerator to perform a media processing function according to a received control command;
- updating a control bit within a register of the register file to indicate whether data is available for one or more data dependent processing elements; and
- requiring the one or more data dependent processing elements to wait to execute instructions until the data it needs to execute the instructions is available in one or more registers.

6. An article of manufacture including a machine readable medium having stored thereon instructions which may be used to program a system to perform a method, comprising:

- providing a register file accessible by a plurality of processing elements of a media signal processor;
- enabling a selected hardware accelerator from a plurality of hardware accelerators according to at least one bit of a register within the register file set by a processing element; and
- granting the processing element ownership over the selected hardware accelerator.

7. The article of manufacture of claim 6, wherein enabling the selected hardware accelerator comprises:

- enabling a processing element to set a bit when the process desires selection of a hardware accelerator; and
- activating the selected hardware accelerator if the bit is set.

8. The article of manufacture of claim 6, wherein enabling the selected hardware accelerator comprises:

designating at least one register within the register file to receive control commands from the plurality of processing elements; and

activating the selected hardware accelerator to perform a media processing function according to a control command detected within the register.

9. The article of manufacture of claim 6, further comprising:

providing a selection unit coupled to the plurality of hardware elements;

designating at least one register within the register file to receive control commands from the plurality of processing elements;

directing the selection unit to provide a processing element with access to a selected hardware element; and

directing the selecting hardware accelerator to perform a media processing function according to a received control command.

10. The article of manufacture of claim 8, wherein activating the selected hardware accelerator comprises:

identifying a processing element having written the control command;

determining, according to the control command, an input data stream for the selected hard accelerator;

determining, according to the control command, an output data stream for the selected hard accelerator;

directing the selecting hardware accelerator to perform a media processing function according to a received control command;

updating a control bit within a register of the register file to indicate whether data is available for one or more data dependent processing elements; and

requiring the one or more data dependent processing elements to wait to execute instructions until the data it needs to execute the instructions is available in one or more registers.

11. A processor, comprising:  
a plurality of processing elements;  
a plurality of hardware accelerators coupled to a selection unit; and  
a register file coupled to the selection unit and the plurality of processing elements, the register file including a plurality of general purpose registers accessible by the plurality of hardware accelerators, the selection unit and the plurality of processing elements, at least one of the general purpose registers including at least one bit to allow a processing element to direct the selection unit to activate a selected hardware accelerator.

12. The processor of claim 11, wherein the plurality of processing elements comprise:

an input processing element coupled to said register file, the input processing element to receive input data; and  
an output processing element coupled to the register file, the output processing element to transmit data.

13. The processor of claim 11, wherein the section unit to receive a control command from a processing element within at least one register of the register file, and activate the selected hardware accelerator to perform a media processing function according to the received control command.

14. The processor of claim 11, wherein the control unit to identify a processing element having written a control command, and set a control bit within a register of the register file to indicate when data is available for the identified processing element from the selected hardware accelerator.

15. The processor of claim 11, wherein a processing element to set a bit when the processing element desires selection of a hardware accelerator and set one more bits to identify one or more data dependent processing elements to prevent the identified processing elements from executing instructions until the one or more bits are reset.

16. The processor of claim 11, wherein the processing element to write a control command to a at least one register within the register file to direct a selected hardware accelerator to perform a media processing function according to the control command and set a control bit to indicate the selected hardware accelerator is in use.

17. The processor of claim 11, wherein a processing element to set one or more control bits within a register of the register file to identify one or more data dependent processing elements to stall the identified processing elements and prohibit execution of instructions until data required by the identified processing elements is available in one or more registers.

18. The processor of claim 11, wherein the hardware accelerators comprise image processing hardware accelerators.

19. The processor of claim 11, wherein the hardware accelerators comprise video processing hardware accelerators.

20. The processor of claim 11, wherein the hardware accelerators comprise audio processing hardware accelerators.

21. A system comprises:

a plurality of media signal processors coupled together via input and output ports to enable data exchange between each media signal processor, the media signal processors including:

a plurality of processing elements;  
a plurality of hardware accelerators coupled to a selection unit;  
a register file coupled to the selection unit and the plurality of processing elements, the register file including a plurality of general purpose registers accessible by the plurality of hardware accelerators and the plurality of processing elements, at least one of the general purpose registers including at least one bit to allow a processing element to activate a selected hardware accelerator via the selection logic unit;  
a memory interface coupled to one or more of the media processors; and  
a random access memory coupled to the memory interface.

22. The system of claim 21, wherein the section unit to receive a control command from a processing element within at least one register of the register file, and activate the selected hardware accelerator to perform a media processing function according to the received control command.

23. The system of claim 21, wherein the control unit to identify a processing element having written a control command and set a control bit within a register of the register file to indicate when data is available for the identified processing element from the selected hardware accelerator.

24. The system of claim 21, wherein a processing element to set a bit when the processing element desires selection of a hardware accelerator and set bits corresponding to one or more data dependent processing elements to prevent the identified processing elements from executing instructions until the one or more bits are reset.

25. The system of claim 21, wherein the processing element to write a control command to a at least one register within the register file to direct a selected hardware accelerator to perform a media processing function according to the written control command and set a control bit to indicate a hardware accelerator is in use.

26. The system of claim 21, wherein a processing element to set one or more control bits within a register of the register file to identify one or more data dependent processing elements to stall the identified processing elements and prohibit execution of an instructions until data required by identified processing elements is available in one or more registers.

28. The system of claim 21, wherein the random access memory (RAM) is a synchronous data random access memory (SDRAM).

29. The system of claim 21, wherein the SDRAM is a double data rate (DDR) SDRAM.